

Description

The Voltage Controlled Solidtron™ (VCS) features high peak current capability and a low on-state voltage drop common to SCR thyristors. Additionally it features extremely high turn-on di/dt capability and virtually no turn-on delay jitter making it ideally suited for a variety of capacitor discharge applications.

The 4-pin F-Pak SM package offers a rugged low inductance interface and allows for installation using automated handling equipment. The package consists of an epoxy filled 4 contact FR4 substrate.

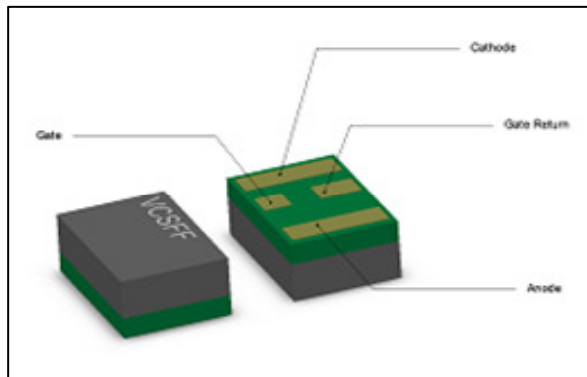
Features

- 1400V Peak Off-State Voltage
- 2.0kA Repetitive Peak Anode Current
- 120kA/uSec di/dt Capability
- 50nSec Turn-On Delay
- Low Loss
- MOS Gate Control

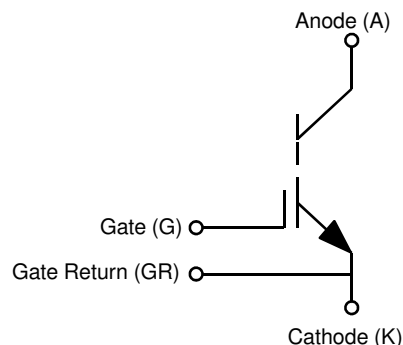
Applications

ESA / EFI

Size - 2



Schematic Symbol



Limiting Characteristics and Ratings

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	V_{DRM}	1400	V
Peak Reverse Voltage	V_{RRM}	-30	V
Off-State Rate of Change of Voltage Immunity ($V_D=1400V$)	dv/dt	5000	V/uSec
Non-repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	I_{ASM}	4800	A
Repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	I_{ASM}	3000	A
Rate of Change of Current	dI/dt	120	kA/uSec
Continuous Gate-Cathode Voltage	V_{GKS}	+/-20	V
Peak Gate-Cathode Voltage	V_{GKM}	+/-25	V
Minimum Gate-Cathode Voltage Required for Guaranteed Off-State	$V_{GK(OFF-MIN)}$	0	V
Maximum Junction Temperature	T_{JM}	125	°C
Maximum Soldering Temperature (Installation)		240	°C

This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

5,521,436	5,446,316	5,105,536	5,209,390	4,958,211	5,206,186	4,857,983	5,082,795	4,644,637
5,585,310	5,557,656	5,777,346	5,139,972	5,111,268	5,757,036	4,888,627	4,980,741	4,374,389
5,248,901	5,564,226	5,446,316	5,103,290	5,260,590	5,777,346	4,912,541	4,941,026	4,750,666
5,366,932	5,517,058	5,577,656	5,028,987	5,350,935	5,995,349	5,424,563	4,927,772	4,429,011
5,497,013	4,814,283	5,473,193	5,304,847	5,640,300	4,801,985	5,399,892	4,739,387	5,293,070
5,532,635	5,135,890	5,166,773	5,569,957	5,184,206	4,476,671	5,468,668	4,648,174	

Performance Characteristics

T _J =25°C unless otherwise specified				Measurements			
Parameters	Symbol	Test Conditions	Min.	Typ.	Max.	Units	
Anode to Cathode Breakdown Voltage	V _(BR)	V _{GK} =-5, I _A =1mA	1400			V	
Anode-Cathode Off-State Current	i _D	V _{GE} =-5V, V _{AK} =1400V	T _C =25°C		1	uA	
			T _C =50°C		3	uA	
			T _C =125°C		5	uA	
Gate-Cathode Leakage Current	I _{GK(lkg)}	V _{GK} =+/-15V	T _C =25°C	4	10	nA	
			T _C =50°C	4	10	nA	
			T _C =125°C	5	10	nA	
Anode-Cathode On-State Voltage	V _T	I _T = 5A, V _{GK} = 5V		1.3		V	
Gate-Cathode Turn-On Threshold Voltage	V _{GK(TH)}	V _{AK} =V _{GK} , I _{AK} =1mA		0.8		V	
Input Capacitance	C _{ISS}	Bias=6V, Freq.=120Hz		1.55		nF	
Turn-on Delay Time	t _{D(ON)}	0.16uF Capacitor Discharge		90		nS	
Rate of Change of Current	di/dt	T _J =25°C, V _{GK} = -5V to +5V		26		kA/uSec	
Peak Anode Current	I _P	V _{AK} =700V, R _G =3.0Ω, L _S =16nH		1660		A	
Rate of Change of Current	di/dt	0.15uF Capacitor Discharge		120		kA/uSec	
Peak Anode Current	I _P	T _J =25°C, V _{GK} = -5V to +5V		6700		A	
		V _{AK} =1200V, R _G =3.0Ω, L _S =6nH					

Typical Performance Curves T_J=25°C unless otherwise specified

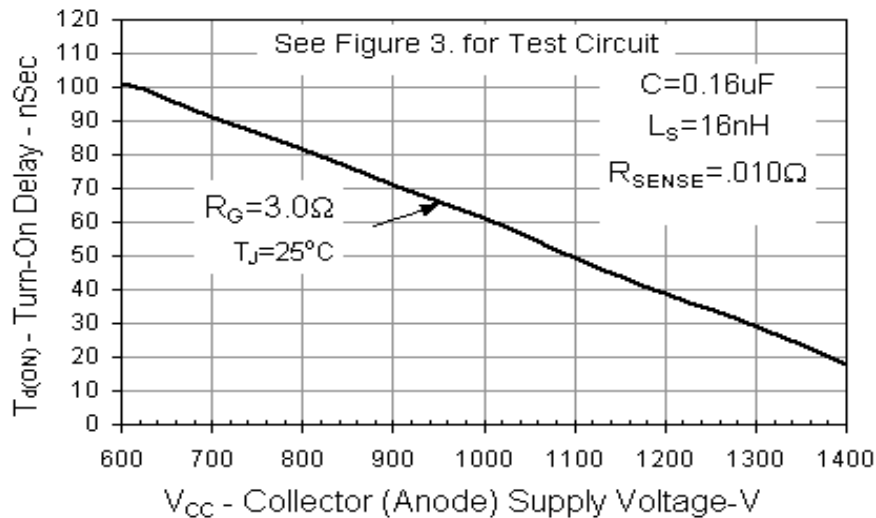


Figure 1. Turn-On Delay Characteristics
 R_G=3.0Ω, T_J=25°C

Typical Performance Curves (Continued)

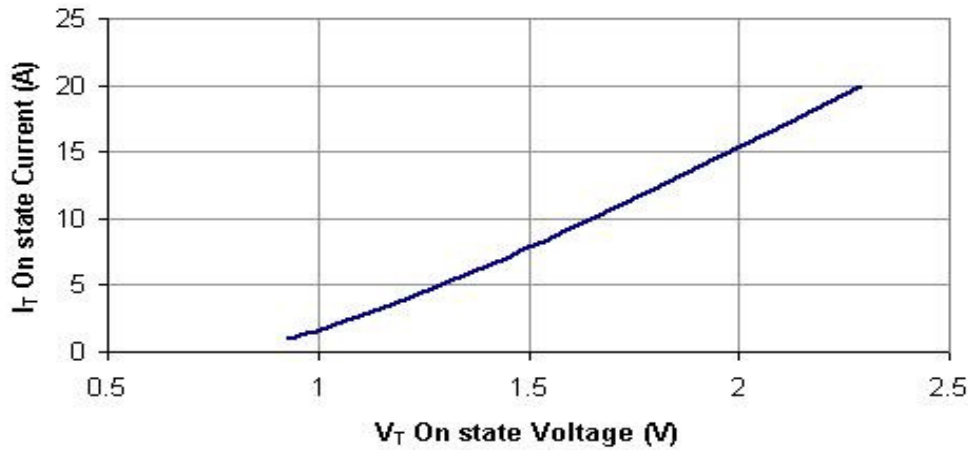
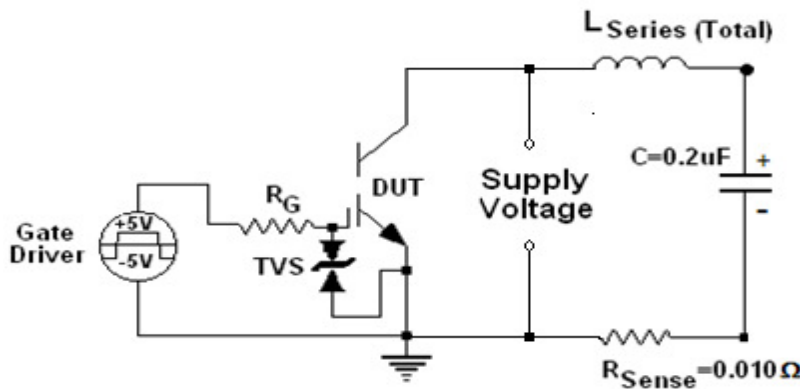


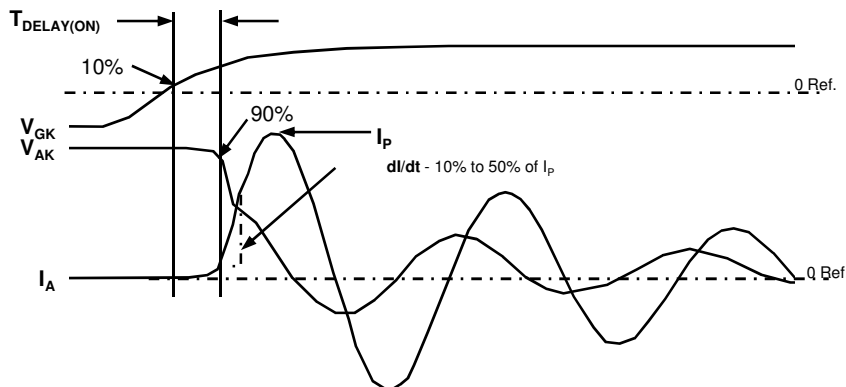
Figure 2 On state characteristics

Test Circuit and Waveforms



- L_{SERIES(TOTAL)} is calculated using $1 / (f 2\pi)^2 C$ where f = frequency of I_A (See Figure 10)
- R_{SENSE} is a calibrated Current Viewing Resistor (CVR)
- TVS - Fairchild SMBJ9V0CA

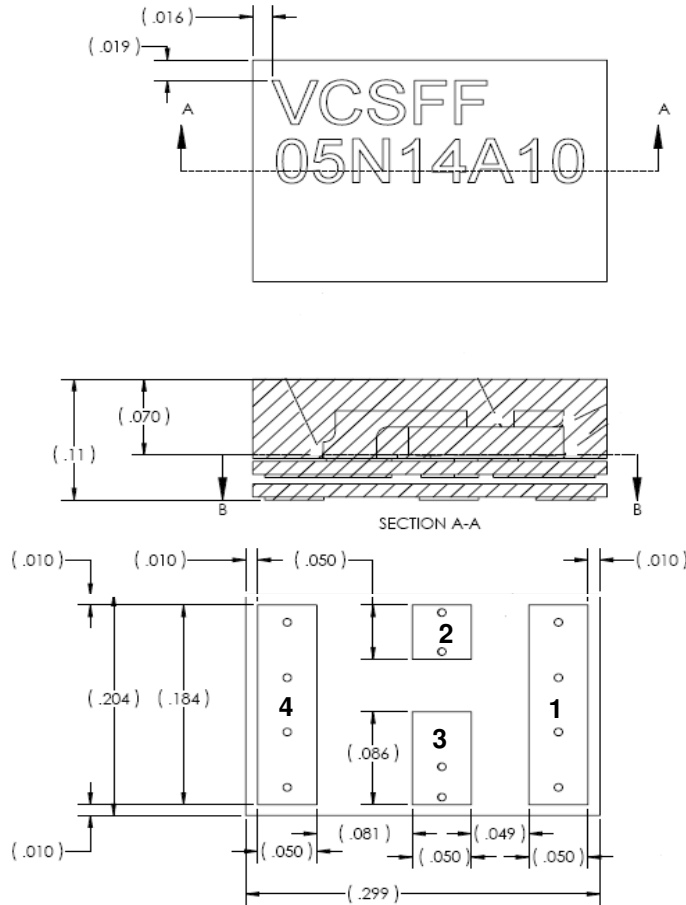
Figure 3. 0.16uF Pulsed Discharge Circuit Schematic



- The waveform shown is representative of one produced using a very low inductance circuit (<10nH).
- V_{GK} is held positive until I_A oscillations have ended (I_A=0).

Figure 4. 0.16uF Pulsed Discharge Circuit Waveforms

Package Dimensions



Pins

1. Cathode
2. Gate
3. Gate Return
4. Anode

All Dimensions are in inches

Figure 5. Critical Package Dimensions and Pin Assignment

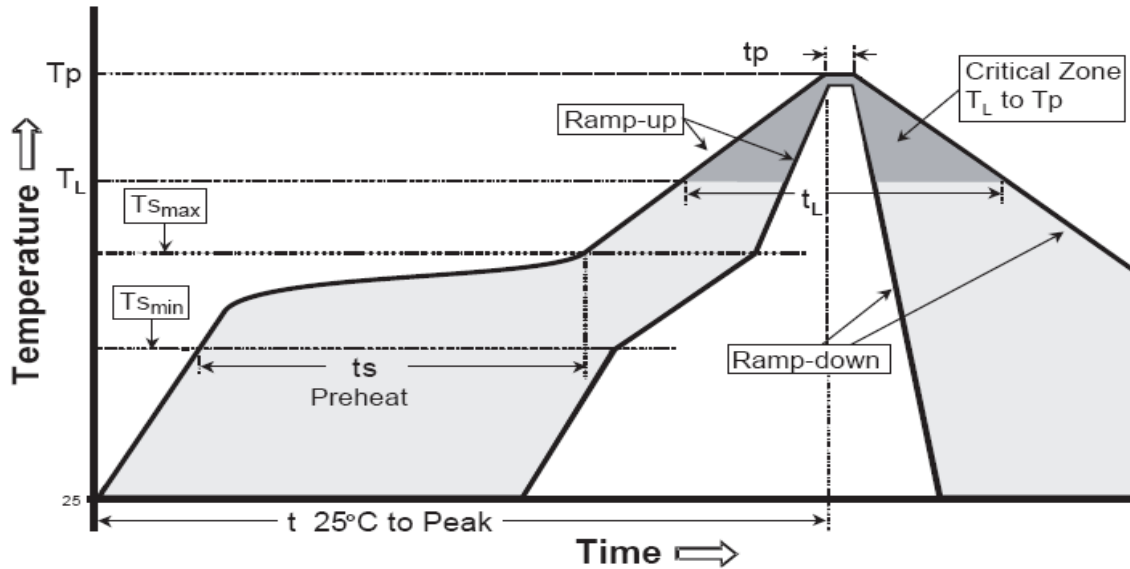
General Handling Precautions

1. Installation reflow temperature should not exceed 240°C or internal package degradation may result.
2. As with all MOS gated devices, proper handling procedures must be observed to prevent electrostatic discharge which may result in permanent damage to the gate of the device
3. Device Storage: Must Comply to MSL Level Six (6)
 Reference IPC/JEDEC J-STD-033 (*)



'ATTENTION OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE DEVICES IN ALL ASSEMBLY AND TEST AREAS'

Recommended Reflow Profile:



IPC-020c-5-1

	Sn-Pb Eutectic assembly
Average Ramp-UP Rate (t _{Smax} to t _p)	3°C/second max.
Preheat	
Temperature Min (t _{Smin})	100°C
Temperature Max (t _{Smax})	150°C
Time (t _{Smin} to t _{Smax})	60-120 seconds
Time maintained above:	
Temperature (t _L)	183°C
Time (t _L)	60-150 seconds
Peak/Classification Temperature (t_p)	240 +0/-5°C
Temperature (t_p)	10-30 seconds
Ramp-Down Rate	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.

Revision History

Rev	Date	EA #	Nature of Change
4	07-09-2010	04242009-NB-0005	Initial Issue