

**Description**

This voltage controlled Solidtron™ (VCS) discharge switch utilizes an n-type MOS-Controlled Thyristor mounted on a ThinPak™, ceramic "chip-scale" hybrid.

The VCS features the high peak current capability and low On-state voltage drop common to SCR thyristors combined with extremely high di/dt capability. This semiconductor is intended for the control of high power circuits with the use of very small amounts of input energy and is ideally suited for capacitor discharge applications.

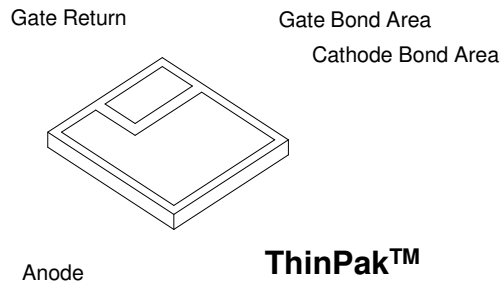
The ThinPak™ Package is a perforated, metalized ceramic substrate attached to the silicon using 302°C solder. An epoxy underfill is applied to protect the high voltage termination from debris. All exterior metal surfaces are tinned with 63pb/37sn solder providing the user with a circuit ready part. It's small size and low profile make it extremely attractive to high di/dt applications where stray series inductance must be kept to a minimum.

**Features**

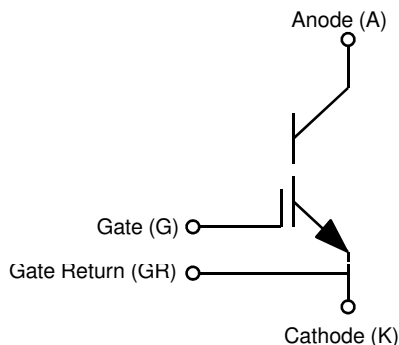
- 1400V Peak Off-State Voltage
- 32A Continuous Rating
- 4kA Surge Current Capability
- >120kA/uSec di/dt Capability
- <100nSec Turn-On Delay
- Low On-State Voltage
- MOS Gated Control
- Low Inductance Package

**Package**

**Size - 4**



**Schematic Symbol**



**Absolute Maximum Ratings**

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	V <sub>DRM</sub>	1400	V
Peak Reverse Voltage	V <sub>RPM</sub>	-5	V
Off-State Rate of Change of Voltage Immunity	dv/dt	5000	V/uSec
Continuous Anode Current at 110°C	I <sub>A110</sub>	32	A
Repetitive Peak Anode Current (Pulse Width=1uSec)	I <sub>ASM</sub>	4000	A
Rate of Change of Current	di/dt	120	kA/uSec
Continuous Gate-Cathode Voltage	V <sub>GKS</sub>	+/-20	V
Peak Gate-Cathode Voltage	V <sub>GKM</sub>	+/-25	V
Minimum Negative Gate-Cathode Voltage Required for Guaranteed Off-State	V <sub>GK(OFF-MIN)</sub>	-5	V
Maximum Junction Temperature	T <sub>JM</sub>	150	°C
Maximum Soldering Temperature (Installation)		260	°C

This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

5,521,436	5,446,316	5,105,536	5,209,390	4,958,211	5,206,186	4,857,983	5,082,795	4,644,637
5,585,310	5,557,656	5,777,346	5,139,972	5,111,268	5,757,036	4,888,627	4,980,741	4,374,389
5,248,901	5,564,226	5,446,316	5,103,290	5,260,590	5,777,346	4,912,541	4,941,026	4,750,666
5,366,932	5,517,058	5,577,656	5,028,987	5,350,935	5,995,349	5,424,563	4,927,772	4,429,011
5,497,013	4,814,283	5,473,193	5,304,847	5,640,300	4,801,985	5,399,892	4,739,387	5,293,070
5,532,635	5,135,890	5,166,773	5,569,957	5,184,206	4,476,671	5,468,668	4,648,174	

Performance Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified			Measurements			
Parameters	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	$V_{(BR)}$	$V_{GK}=-5, I_A=1\text{mA}$	1400			V
Anode-Cathode Off-State Current	$i_D$	$V_{GE}=-5\text{V}, V_{AK}=1200\text{V}$	$T_C=25^\circ\text{C}$	<1.0	10	$\mu\text{A}$
			$T_C=150^\circ\text{C}$	<10	100	$\mu\text{A}$
Gate-Cathode Turn-On Threshold Voltage	$V_{GK(TH)}$	$V_{AK}=V_{GK}, I_{AK}=1\text{mA}$		1		V
Gate-Cathode Leakage Current	$I_{GK(IG)}$	$V_{GK}=\pm 20\text{V}$			500	nA
Anode-Cathode On-State Voltage	$V_T$	$I_T=32\text{A}, V_{GK}=+5\text{V}$ (See Figures 1,2 & 3)	$T_C=25^\circ\text{C}$	1.5	2.0	V
			$T_C=150^\circ\text{C}$	1.3	1.5	V
Input Capacitance	$C_{ISS}$			6		nF
Turn-on Delay Time	$t_{D(ON)}$	0.2 $\mu\text{F}$ Capacitor Discharge		50	100	nS
Rate of Change of Current	$di/dt$	$T_J=25^\circ\text{C}, V_{GK}=-5\text{V to }+5\text{V}$		75		kA/ $\mu\text{Sec}$
Peak Anode Current	$I_P$	$V_{AK}=800\text{V}, R_G=4.7\Omega$		3500		A
Discharge Event Energy	$E_{DIS}$	$L_S=7\text{nH}$ (See Figures 4,5 & 6)		32		mJ
Turn-on Delay Time	$t_{D(ON)}$	0.2 $\mu\text{F}$ Capacitor Discharge		50	100	nS
Rate of Change of Current	$di/dt$	$T_J=150^\circ\text{C}, V_{GK}=-5\text{V to }+5\text{V}$		110		kA/ $\mu\text{Sec}$
Peak Anode Current	$I_P$	$V_{AK}=1200\text{V}, R_G=4.7\Omega$	4000			A
Discharge Event Energy	$E_{DIS}$	$L_S=7\text{nH}$ (See Figures 4,5 & 6)		70		mJ
Junction to Case Thermal Resistance	$R_{\theta JC}$	Anode (bottom) side cooled (Note 1.)		0.08		$^\circ\text{C/W}$
Junction to Case Thermal Resistance	$R_{\theta JC}$	Cathode-Gate (top) side cooled (Note 2.)		1.5		$^\circ\text{C/W}$

Notes:

- Case Exterior Assumed to be 0.002" of 63sn/37pb solder applied directly to Anode. (See Figure 7.)
- Case Exterior Assumed to be 0.002" of 63sn/37pb solder applied directly to cathode bond area of thinPak. (See Figure 7.)

**Typical Performance Curves** (unless otherwise specified)

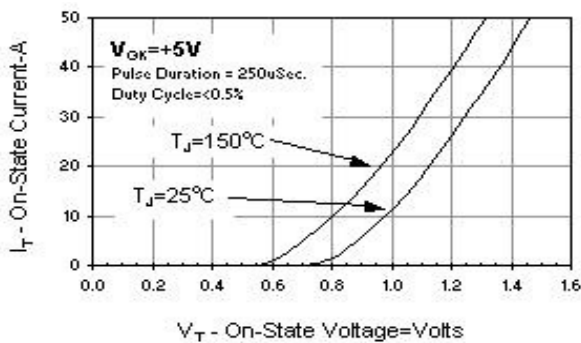


Figure 1. On-State Characteristics

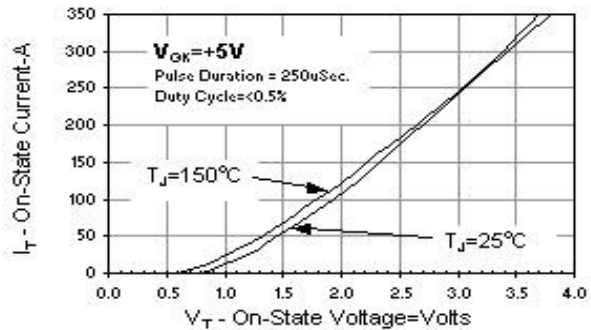


Figure 2. On-State Characteristics

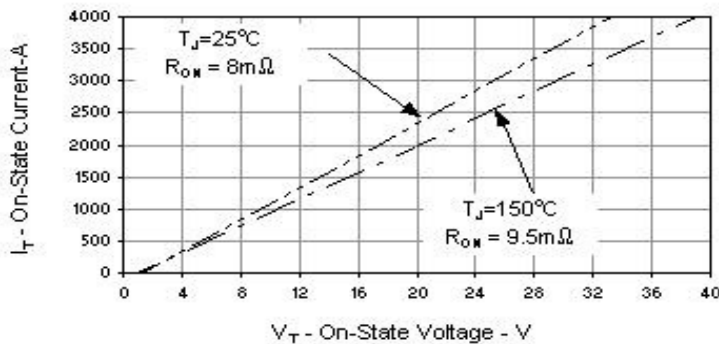
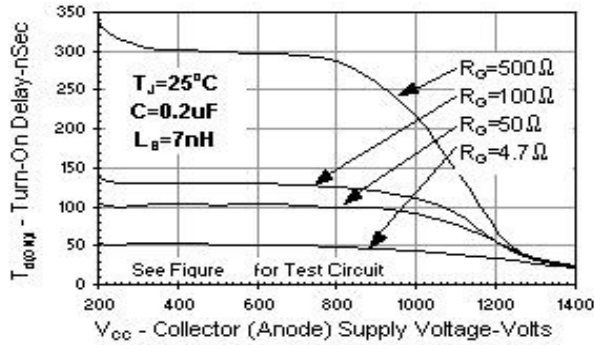
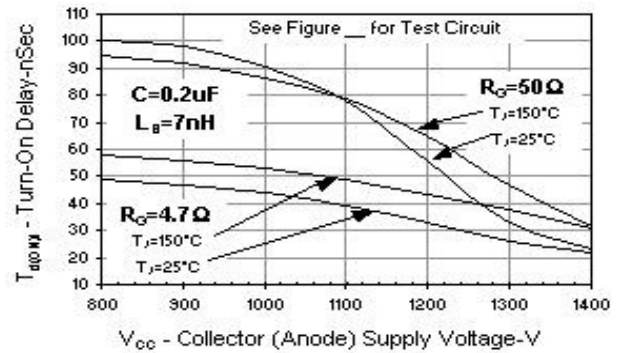


Figure 3. Predicted High Current On-State Characteristics:

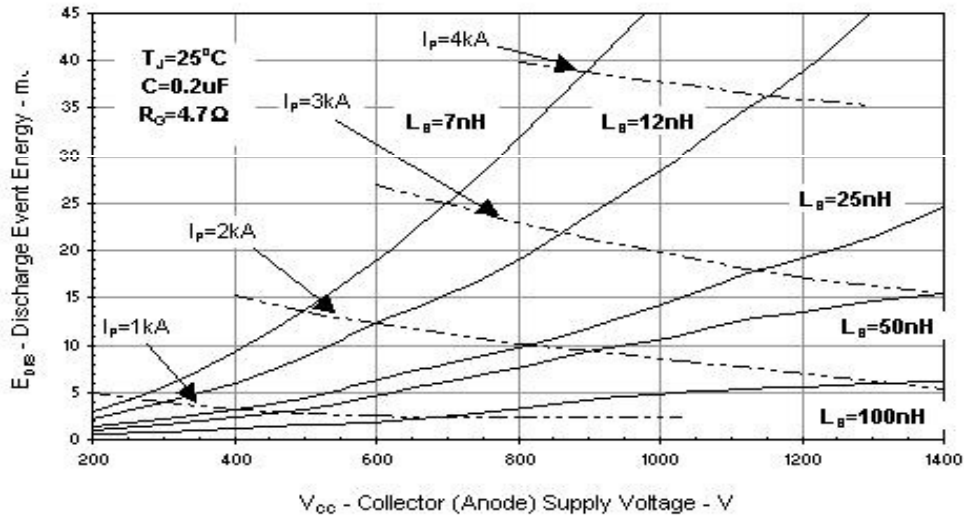
**Typical Performance Curves (Continued)**



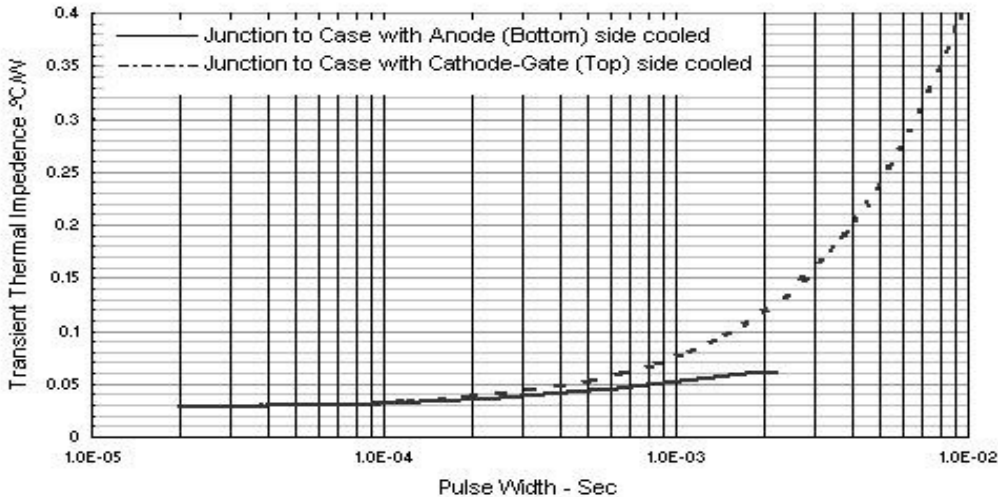
**Figure 4.** Turn-On Delay Characteristics  
 $R_G = 4.7\Omega - 500\Omega$ ,  $T_J = 25^\circ\text{C}$



**Figure 5.** Turn-On Delay Characteristics  
 $R_G = 4.7\Omega \text{ \& } 50\Omega$ ,  $T_J = 25^\circ\text{C} \text{ \& } 150^\circ\text{C}$



**Figure 6.** 0.2uF Discharge Pulse Performance Characteristics (See Figure 9.)



**Figure 7.** Transient Thermal Impedance Response

**Typical Performance Curves (Continued)**

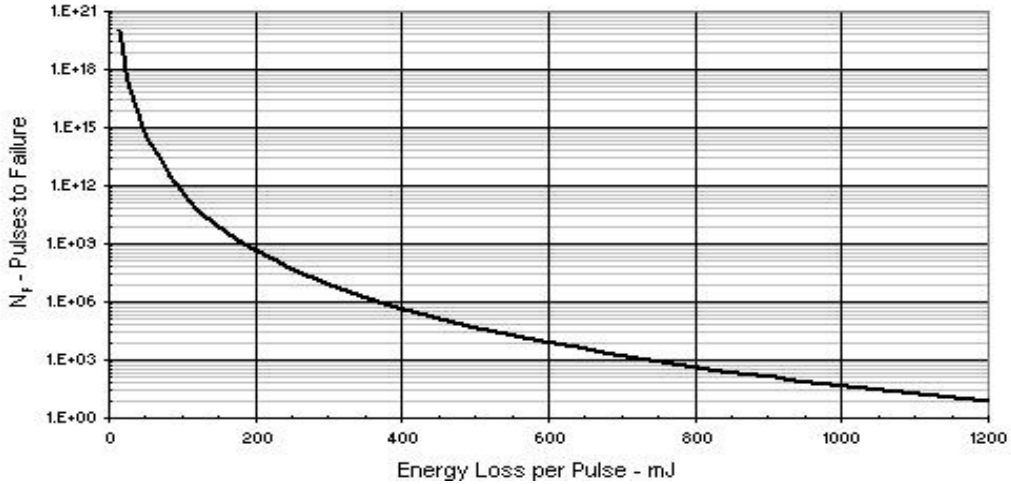
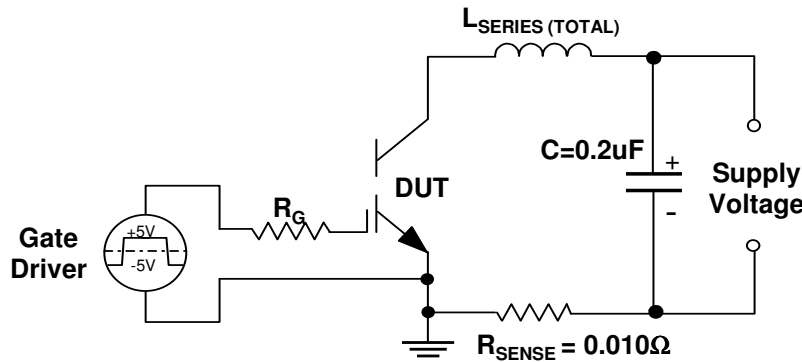


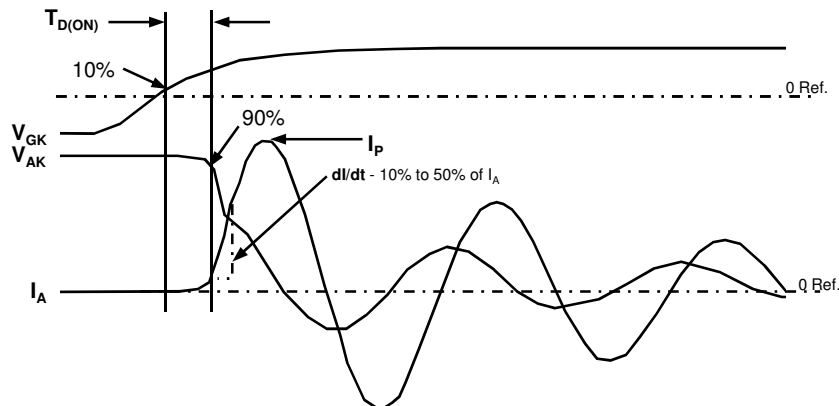
Figure 8. Pulses to Failure (Pulse Widths < 100uSec)

**Test Circuit and Waveforms**



- $L_{SERIES(TOTAL)}$  is calculated using  $1 / (f 2\pi)^2 C$  where  $f$  = frequency of  $I_A$  (See Figure 10)
- $R_{SENSE}$  is a calibrated Current Viewing Resistor (CVR)

Figure 9. 0.2uF Pulsed Discharge Circuit Schematic



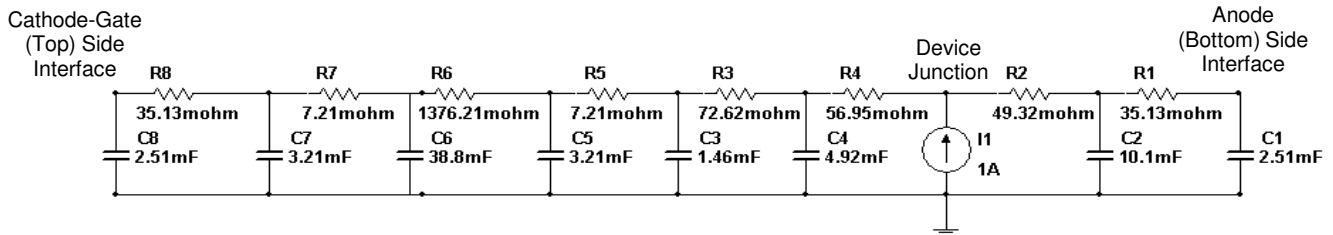
- The waveform shown is representative of one produced using a very low inductance circuit (<10nH).
- $V_{GK}$  is held positive until  $I_A$  oscillations have ended ( $I_A=0$ ).

Figure 10. 0.2uF Pulsed Discharge Circuit Waveforms

**Application Notes**

**A1. Junction Temperature Calculation**

The figure below shows a lump model of the thermal properties of the size 4 thinPak packaged VCS, from the 2-mil solder on the top of the lid on the left to the 2-mil solder on the bottom of the device on the right. By adding the user's lump model of the rest of the thermal system the user can calculate the junction and case temperature rise under any operating condition.



**A2. Calculation of Pulses to Failure for Intermediate/Long Pulse Widths**

The user may calculate the Number of Pulses to failure ( $N_F$ ) for long to intermediate pulse widths (not covered in the typical performance curve section) by applying the junction temperature rise ( $dT$ ), calculated as described in A1, to the formula  $N_F = (300/dT)^9$ .

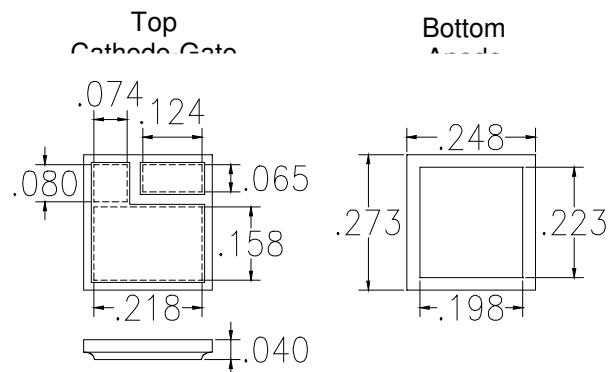
**A3. Use of Gate Return Bond Area.**

The MCT was designed for high di/dt applications. An independent cathode connection or "Gate Return Bond Area" was provided to minimize the effects of rapidly changing Anode-Cathode current on the Gate control voltage, ( $V=L \cdot di/dt$ ). It is therefore, critical that the user utilize the Gate Return Bond Area as the point at which the gate driver reference (return) is attached to the VCS device.

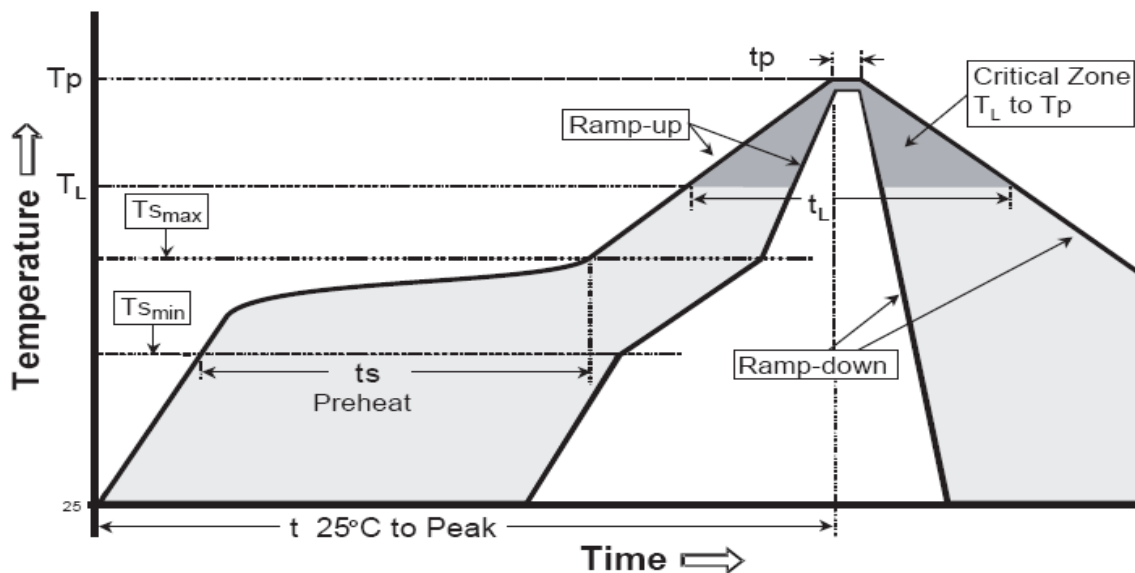
**Packaging and Handling**

1. All metal surfaces are tinned using 63pb/37sn solder.
2. Installation reflow temperature should not exceed 260°C or internal package degradation may result.
3. Package may be cooled from either top or bottom (See Figure 7)
4. As with all MOS gated devices, proper handling procedures must be observed to prevent electrostatic discharge which may result in permanent damage to the gate of the device

**Package Dimensions**



**Recommended Reflow Profile:**



IPC-020C-5-1

	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate ( $t_{smax}$ to $t_p$ )	3°C/second max.	3°C/second max.
Preheat		
Temperature Min ( $t_{smin}$ )	100°C	150°C
Temperature Max ( $t_{smax}$ )	150°C	200°C
Time ( $t_{smin}$ to $t_{smax}$ )	60-120 seconds	60-180 seconds
Time maintained above:		
Temperature ( $t_L$ )	183°C	217°C
Time ( $t_L$ )	60-150 seconds	60-150 seconds
Peak/Classification Temperature ( $t_p$ )	240 +0/-5°C	260 +0°C
Temperature ( $t_p$ )	10-30 seconds	20-40 seconds
Ramp-Down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

**Revision History**

Rev	Date	EA #	Nature of Change
2	07-10-2008	04242009-NB-0007	Initial Issue