

**Description**

This voltage controlled Solidtron™ (VCS) discharge switch utilizes an n-type MOS-Controlled Thyristor mounted in a five lead TO-247 plastic package.

The VCS features the high peak current capability and low On-state voltage drop common to SCR thyristors combined with extremely high di/dt capability. This semiconductor is intended for the control of high power circuits with the use of very small amounts of input energy and is ideally suited for capacitor discharge applications.

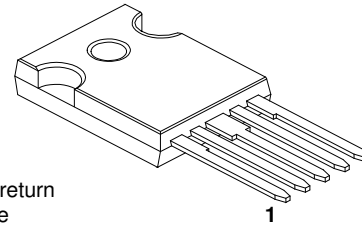
The industry standard TO-247 package allows for integration of the Solidtron using automated insertion equipment.

**Features**

- 1400V Peak Off-State Voltage
- 32A Continuous Rating
- 4kA Surge Current Capability
- >100kA/uSec di/dt Capability
- <100nSec Turn-On Delay
- Low On-State Voltage
- MOS Gated Control
- Low Inductance Package

**Package**

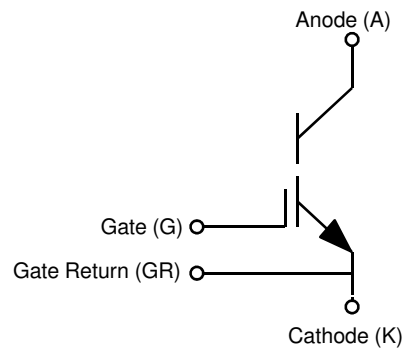
Size - 4



- Pin 1 : Gate
- Pin 2 : Gate return
- Pin 3 : Anode
- Pin 4 : Cathode
- Pin 5 : Cathode

**5 Lead TO-247**

**Schematic Symbol**



**Absolute Maximum Ratings**

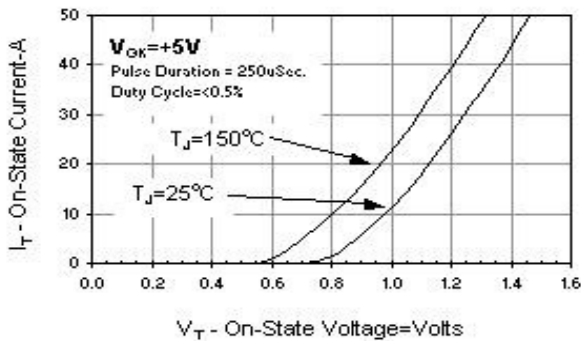
	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	V <sub>DRM</sub>	1400	V
Peak Reverse Voltage	V <sub>RRM</sub>	-5	V
Off-State Rate of Change of Voltage Immunity	dv/dt	5000	V/uSec
Continuous Anode Current at 110°C	I <sub>A110</sub>	32	A
Repetitive Peak Anode Current (Pulse Width=1uSec)	I <sub>ASM</sub>	4000	A
Rate of Change of Current	di/dt	150	kA/uSec
Continuous Gate-Cathode Voltage	V <sub>GKS</sub>	+/-20	V
Peak Gate-Cathode Voltage	V <sub>GKM</sub>	+/-25	V
Minimum Negative Gate-Cathode Voltage Required for Garanteed Off-State	V <sub>GK(OFF-MIN)</sub>	-5	V
Maximum Junction Temperature	T <sub>JM</sub>	150	°C
Maximum Soldering Temperature (Installation)		260	°C

This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

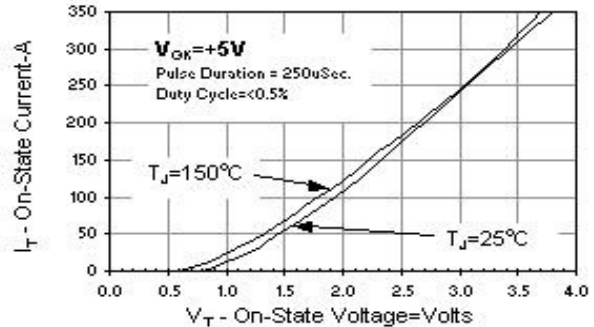
5,521,436	5,446,316	5,105,536	5,209,390	4,958,211	5,206,186	4,857,983	5,082,795	4,644,637
5,585,310	5,557,656	5,777,346	5,139,972	5,111,268	5,757,036	4,888,627	4,980,741	4,374,389
5,248,901	5,564,226	5,446,316	5,103,290	5,260,590	5,777,346	4,912,541	4,941,026	4,750,666
5,366,932	5,517,058	5,577,656	5,028,987	5,350,935	5,995,349	5,424,563	4,927,772	4,429,011
5,497,013	4,814,283	5,473,193	5,304,847	5,640,300	4,801,985	5,399,892	4,739,387	5,293,070
5,532,635	5,135,890	5,166,773	5,569,957	5,184,206	4,476,671	5,468,668	4,648,174	

Performance Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified			Measurements			
Parameters	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	$V_{(BR)}$	$V_{GK}=-5, I_A=1\text{mA}$	1400			V
Anode-Cathode Off-State Current	$i_D$	$V_{GE}=5\text{V}, V_{AK}=1200\text{V}$	$T_C=25^\circ\text{C}$	<10	100	$\mu\text{A}$
			$T_C=150^\circ\text{C}$	250	1000	$\mu\text{A}$
Gate-Cathode Turn-On Threshold Voltage	$V_{GK(TH)}$	$V_{AK}=V_{GK}, I_{AK}=1\text{mA}$		0.7		V
Gate-Cathode Leakage Current	$I_{GK(IKG)}$	$V_{GK}=\pm 20\text{V}$			500	nA
Anode-Cathode On-State Voltage	$V_T$	$I_T=32\text{A}, V_{GK}=+5\text{V}$ (See Figures 1,2 & 3)	$T_C=25^\circ\text{C}$	1.5	2.0	V
			$T_C=150^\circ\text{C}$	1.3	1.5	V
Input Capacitance	$C_{ISS}$			6		nF
Turn-on Delay Time	$t_{D(ON)}$	0.2 $\mu\text{F}$ Capacitor Discharge		50	100	nS
Rate of Change of Current	$di/dt$	$T_J=25^\circ\text{C}, V_{GK}= -5\text{V to } +5\text{V}$		75		kA/ $\mu\text{Sec}$
Peak Anode Current	$I_P$	$V_{AK}=800\text{V}, R_G=4.7\Omega$		3500		A
Discharge Event Energy	$E_{DIS}$	$L_S= 7\text{nH}$ (See Figures 4,5 & 6)		32		mJ
Turn-on Delay Time	$t_{D(ON)}$	0.2 $\mu\text{F}$ Capacitor Discharge		50	100	nS
Rate of Change of Current	$di/dt$	$T_J=150^\circ\text{C}, V_{GK}= -5\text{V to } +5\text{V}$		110		kA/ $\mu\text{Sec}$
Peak Anode Current	$I_P$	$V_{AK}=1200\text{V}, R_G=4.7\Omega$	4000			A
Discharge Event Energy	$E_{DIS}$	$L_S= 7\text{nH}$ (See Figures 4,5 & 6)		70		mJ
Junction to Case Thermal Resistance	$R_{\theta JC}$	Anode (bottom) side cooled (Note 1.)		0.08		$^\circ\text{C/W}$

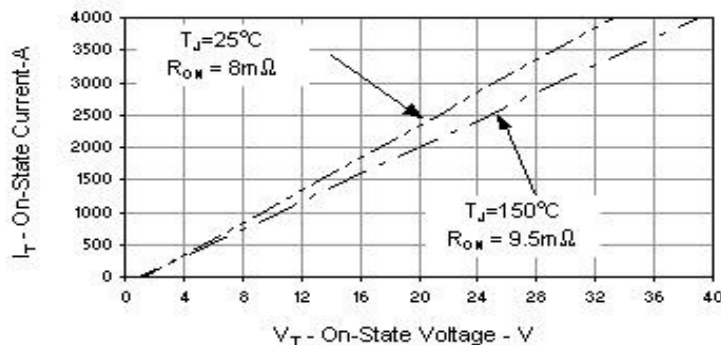
**Typical Performance Curves** (unless otherwise specified)



**Figure 1.** On-State Characteristics

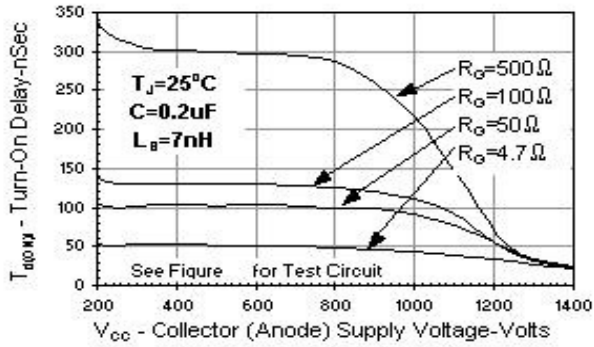


**Figure 2.** On-State Characteristics

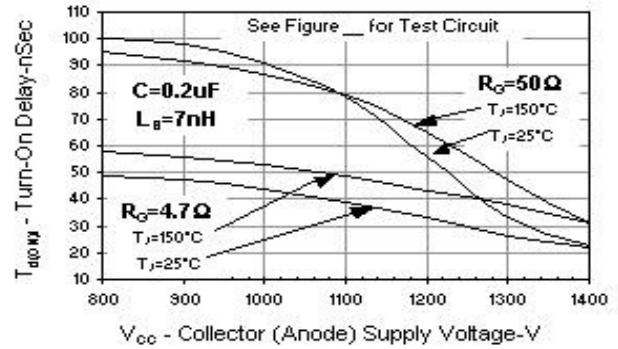


**Figure 3.** Predicted High Current On-State Characteristics

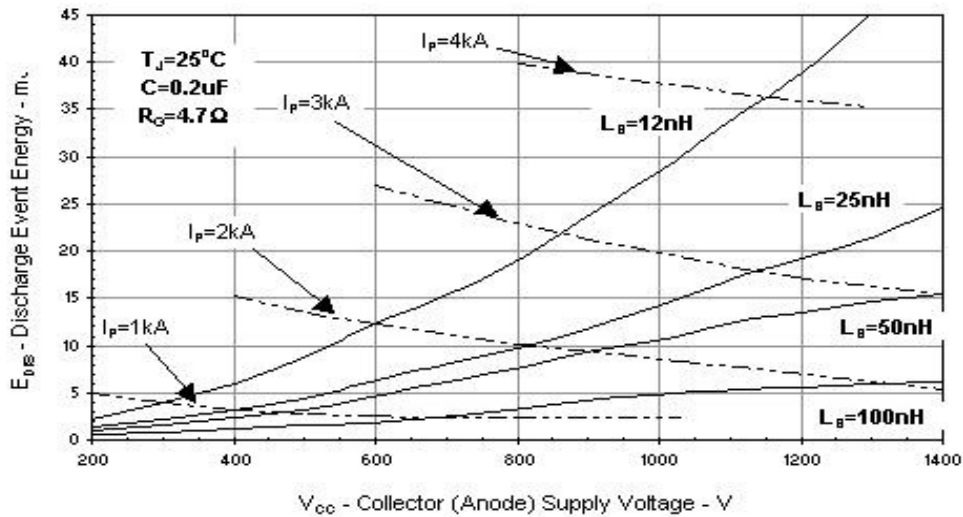
**Typical Performance Curves (Continued)**



**Figure 4.** Turn-On Delay Characteristics  
 $R_G=4.7\Omega - 500\Omega$ ,  $T_J=25^\circ\text{C}$

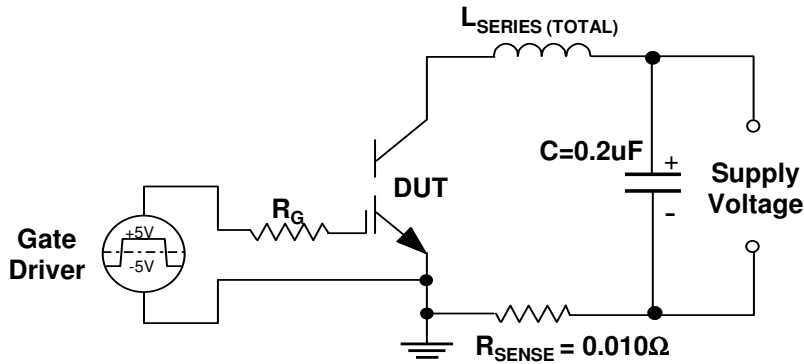


**Figure 5.** Turn-On Delay Characteristics  
 $R_G=4.7\Omega$  &  $50\Omega$ ,  $T_J=25^\circ\text{C}$  &  $150^\circ\text{C}$



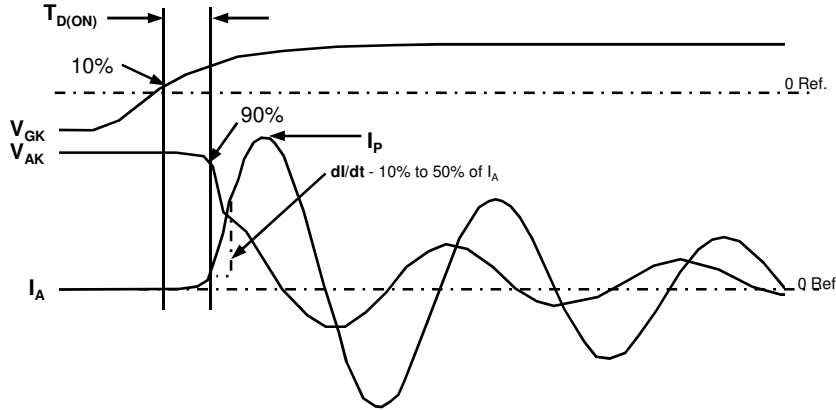
**Figure 6.** 0.2uF Discharge Pulse Performance Characteristics (See Figure 9.)

**Test Circuit and Waveforms**



- $L_{SERIES(TOTAL)}$  is calculated using  $1 / (f 2\pi)^2 C$  where  $f$  = frequency of  $I_A$  (See Figure 10)
- $R_{SENSE}$  is a calibrated Current Viewing Resistor (CVR)

**Figure 9.** 0.2uF Pulsed Discharge Circuit Schematic



- The waveform shown is representative of one produced using a very low inductance circuit (<10nH).
- $V_{GK}$  is held positive until  $I_A$  oscillations have ended ( $I_A=0$ ).

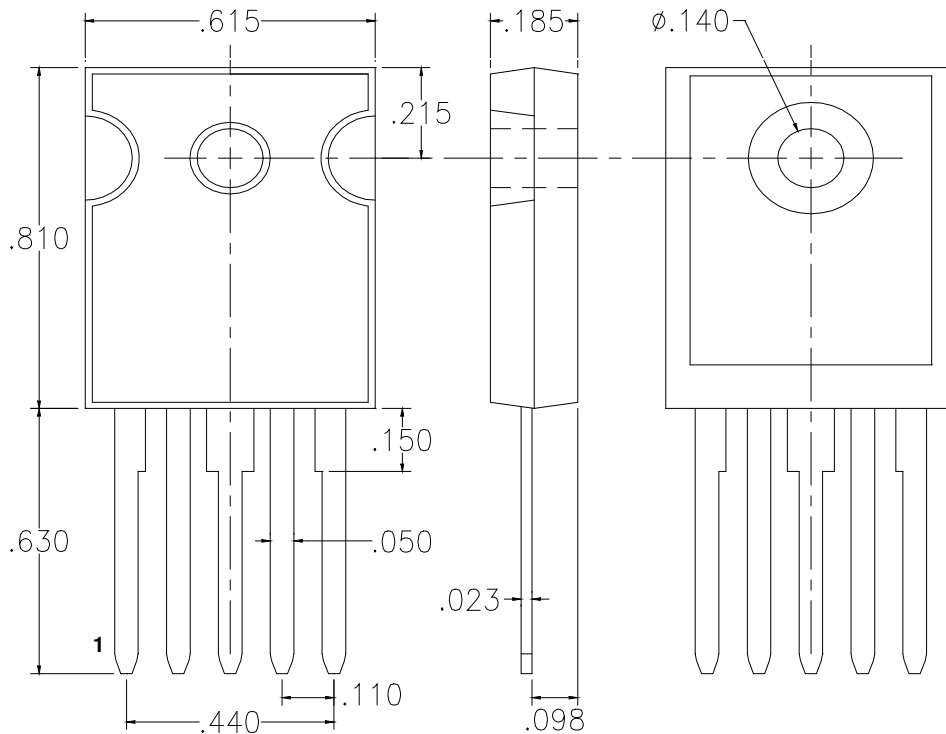
**Figure 10.** 0.2uF Pulsed Discharge Circuit Waveforms

### Application Notes

#### A1. Use of Gate Return

The VCS was designed for high di/dt applications. An independent cathode connection for use as "gate return" is provided on pin 2 to minimize the effects of rapidly changing Anode-Cathode current on the Gate control voltage, ( $V=L \cdot di/dt$ ). It is therefore, critical that the user utilize the Gate Return as the point at which the gate driver reference (return) is attached to the VCS device.

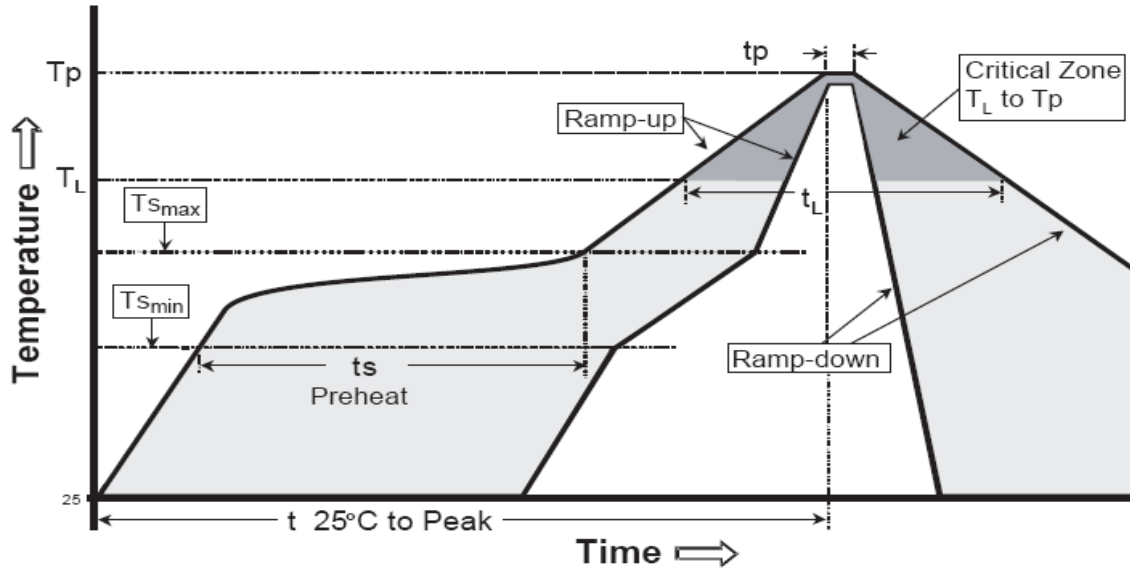
### Packaging and Handling



Pin 1 : Gate  
 Pin 2 : Gate return  
 Pin 3 : Anode  
 Pin 4 : Cathode  
 Pin 5 : Cathode

As with all MOS gated devices, proper handling procedures must be observed to prevent electrostatic discharge which may result in permanent damage to the gate of the device

**Recommended Reflow Profile:**



IPC-020c-5-1

Profile Feature	Sn-Pb Eutectic Assembly
<b>Average Ramp-Up Rate</b> ( $T_{Smax}$ to $T_p$ )	3 °C/second max.
<b>Preheat</b>	
- Temperature Min ( $T_{Smin}$ )	100 °C
- Temperature Max ( $T_{Smax}$ )	150 °C
- Time ( $t_{Smin}$ to $t_{Smax}$ )	60-120 seconds
<b>Time maintained above:</b>	
- Temperature ( $T_L$ )	183 °C
- Time ( $t_L$ )	60-150 seconds
Peak/Classification Temperature ( $T_p$ )	225 + 0/-5 °C
<b>Time within 5 °C of actual Peak</b>	
Temperature ( $t_p$ )	10-30 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.

**Revision History**

Rev	Date	EA #	Nature of Change
0	12-19-2007	04242009-NB-0010	Initial Issue