Doc. No. S5002 Rev 1.0 5/21/04

Current Controlled Solidtron – Trigger Circuits

Contributors: J. Mookken & K. Brandmier
Silicon Power Corp., 175 Great Valley Parkway, Malvern PA.

1.0 Introduction

Driving Voltage Controlled Solidtrons (VCS) is similar to driving power MOSFETs or IGBT devices, but with a few important differences. VCS devices require a negative gate bias to guarantee Off-State; additionally they are also latching devices. Another important difference is that VCS devices cannot hard turn-off high levels of switch conduction current (anode-cathode current). For example, the SMCTTA32N14A10 devices can turn-on up to 4kA for a short time (~ 1uS), but can only force commutate (turn-off) 30A of switch conduction current. Once a VCS is triggered and the device will almost immediately latch until either the current self-commutates and a negative gate bias is applied or force commutated with a negative gate bias at low conduction current levels.

2.0 Pulse-transformer trigger design

A preferred method of isolation, a pulse transformer may be used to predictably and reliably trigger the Thyristor. This gating method allows the user to easily connect the devices in parallel or series (See Fig. A1.2 for series example).

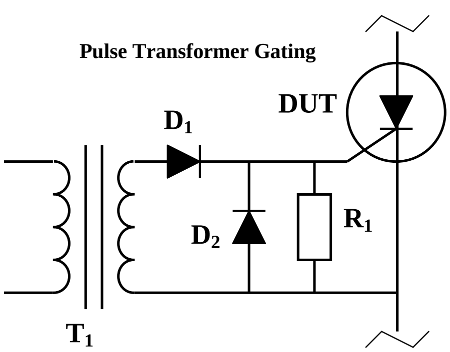

Figure 1. A pulse transformer trigger circuit.

T1 - Method of electrically isolating the device from control circuitry. Pulse X-former insulation characteristic must be selected based on application requirements.

R1 (or RGK) - Serves as a keep-off resistor, shunting dv/dt induced, capacitively coupled Anode-Gate current to the Cathode. The lower the value of R1, the better the dv/dt immunity of the sub-circuit. In the event R1 must be increased to the point where it's resistance compromises the dv/dt requirement of the application, a low voltage capacitor (.1-.2uF) may be placed in parallel to provide a more responsive shunt path; however, the added capacitance will require more charge be delivered to satisfy the turn-on requirements outlined in the simplified theory of operation.

D1 & D2 - Current steering diodes. Reverse gate current increases the impedance of the device ("attempted turn-off"). Reverse gate current experienced during a high current discharge event may permanently damage the device. D1 restricts the direction of current flow through the secondary while D2 provides a "free-wheeling" or holding path to the gate.

It is highly recommended that the components listed above, specifically R1 and D2 be placed in as close physical/electrical proximity to the device as the application will allow. Parasitic inductance in series with the Gate to Cathode shunt path will also compromise the dv/dt immunity of the device.

2.1 Theory of Operation

A current pulse supplied to the primary of T1 induces a current into the secondary of T1. Current supplied by the T1 secondary forward biases D1 supplying current through R1; thus, developing voltage across R1 until the gate of the Thyristor is forward biased (~0.7V). Current is then supplied to the Gate of the Thyristor until turn-on (latchedon) is achieved. Following the discharge event, once the Thyristor current reaches zero and it's stored charge is cleared (Storage Time) the circuit is reset and Anode voltage may be reapplied.

Example: Turn-on will occur with R1=5 ohms, IT1-S =/> 140mA

It is recommended that T1 secondary current (IT1-S) =/> 0.7V / R1 be supplied for approximately 2uSec. Device turn-on delay (TD-ON) is typically less than 200nSec.

Although IT1-S = 0.7V / R1 is sufficient to turn the device on, we typically recommend, where possible, IT1-S =/ >500mA, Pulse Duration =/> 5uSec with R1= 10 ohms.

.

For additional Questions:
John Mookken
Solidtron@siliconpower.com
866 TO SOLID