

**Description**

This voltage controlled Solidtron™ (VCS) discharge switch utilizes an n-type MOS-Controlled Thyristor.

The VCS features the high peak current capability and low On-state voltage drop common to SCR thyristors combined with extremely high di/dt capability. This semiconductor is intended for the control of high power circuits with the use of very small amounts of input energy and is ideally suited for capacitor discharge applications.

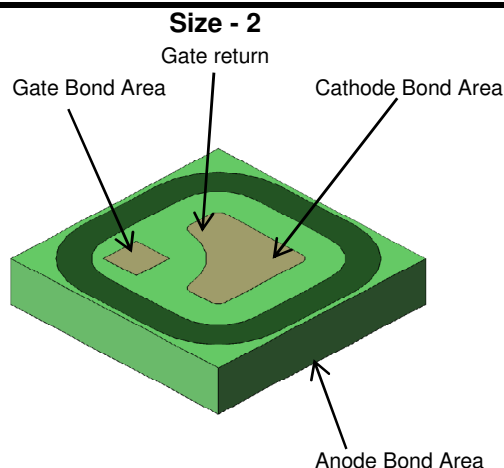
All bond areas are metallized with solderable metal surfaces providing the user with a solderable device. It's small size and low profile make it extremely attractive to high di/dt applications where stray series inductance must be kept to a minimum.

**Features**

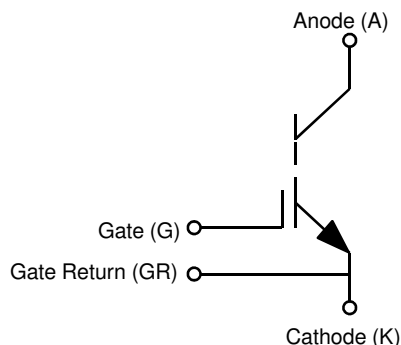
- 1400V Peak Off-State Voltage
- 2.0kA Repetitive Peak Anode Current
- >50kA/uSec di/dt Capability
- 50nSec Turn-On Delay
- Low Loss
- MOS Gate Control

**Applications**

ESA / EFI



**Schematic Symbol**



**Limiting Characteristics and Ratings**

	SYMBOL	VALUE	UNITS
Peak Off-State Voltage	$V_{DRM}$	1400	V
Peak Reverse Voltage	$V_{RRM}$	-5	V
Off-State Rate of Change of Voltage Immunity ( $V_D=1400V$ )	dv/dt	5000	V/uSec
Non-repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	$I_{ASM}$	2000	A
Repetitive Peak Anode Current (Sinusoid Pulse Duration=250nSec)	$I_{ASM}$	1800	A
Rate of Change of Current	di/dt	50	kA/uSec
Continuous Gate-Cathode Voltage	$V_{GKS}$	+/-15	V
Peak Gate-Cathode Voltage	$V_{GKM}$	+/-18	V
Minimum Negative Gate-Cathode Voltage Required for Guaranteed Off-State	$V_{GK(OFF-MIN)}$	-5	V
Maximum Junction Temperature	$T_{JM}$	125	°C
Maximum Soldering Temperature (Installation)		260	°C

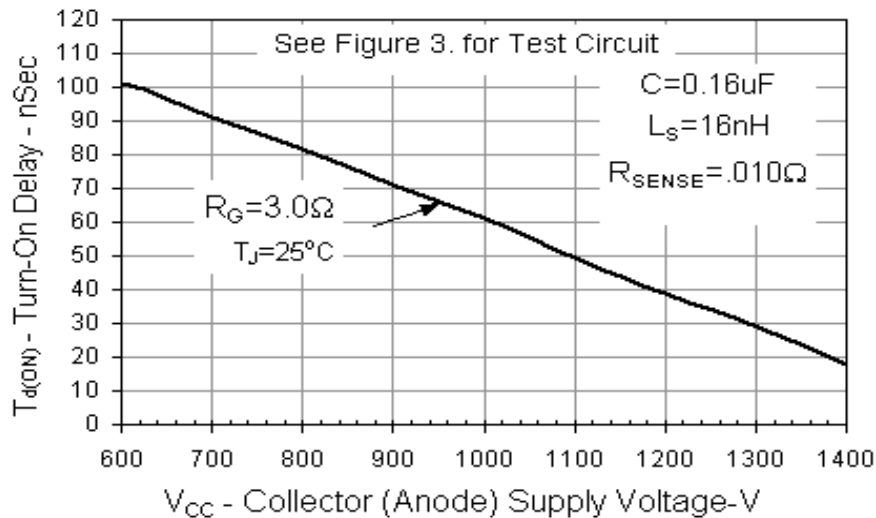
This **SILICON POWER** product is protected by one or more of the following U.S. Patents:

5,521,436	5,446,316	5,105,536	5,209,390	4,958,211	5,206,186	4,857,983	5,082,795	4,644,637
5,585,310	5,557,656	5,777,346	5,139,972	5,111,268	5,757,036	4,888,627	4,980,741	4,374,389
5,248,901	5,564,226	5,446,316	5,103,290	5,260,590	5,777,346	4,912,541	4,941,026	4,750,666
5,366,932	5,517,058	5,577,656	5,028,987	5,350,935	5,995,349	5,424,563	4,927,772	4,429,011
5,497,013	4,814,283	5,473,193	5,304,847	5,640,300	4,801,985	5,399,892	4,739,387	5,293,070
5,532,635	5,135,890	5,166,773	5,569,957	5,184,206	4,476,671	5,468,668	4,648,174	

**Performance Characteristics**

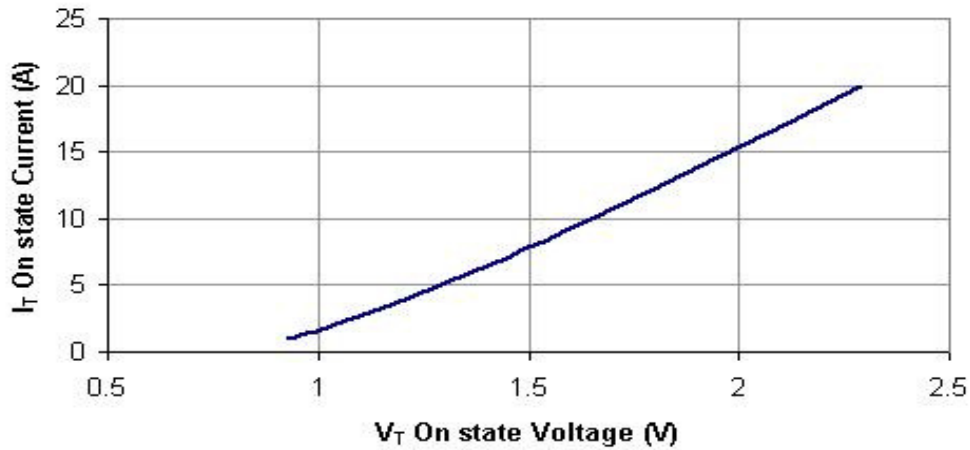
T <sub>J</sub> =25°C unless otherwise specified			Measurements			
Parameters	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Anode to Cathode Breakdown Voltage	V <sub>(BR)</sub>	V <sub>GK</sub> =-5, I <sub>A</sub> =1mA	1400			V
Anode-Cathode Off-State Current	i <sub>D</sub>	V <sub>GE</sub> =-5V, V <sub>AK</sub> =1400V	T <sub>C</sub> =25°C		1	uA
			T <sub>C</sub> =50°C		3	uA
			T <sub>C</sub> =125°C		5	uA
Gate-Cathode Leakage Current	I <sub>GK(lkg)</sub>	V <sub>GK</sub> =+/-15V	T <sub>C</sub> =25°C	4	10	nA
			T <sub>C</sub> =50°C	4	10	nA
			T <sub>C</sub> =125°C	5	10	nA
Anode-Cathode On-State Voltage	V <sub>T</sub>	I <sub>T</sub> = 5A, V <sub>GK</sub> = 5V		1.3		V
Gate-Cathode Turn-On Threshold Voltage	V <sub>GK(TH)</sub>	V <sub>AK</sub> =V <sub>GK</sub> , I <sub>AK</sub> =1mA	0.8	0.8	1.2	V
Input Capacitance	C <sub>ISS</sub>	Bias=6V, Freq.=120Hz		1.55		nF
Turn-on Delay Time	t <sub>D(ON)</sub>	0.16uF Capacitor Discharge		90		nS
Rate of Change of Current	di/dt	T <sub>J</sub> =25°C, V <sub>GK</sub> = -5V to +5V		26		kA/uSec
Peak Anode Current	I <sub>P</sub>	V <sub>AK</sub> =700V, R <sub>G</sub> =3.0Ω, L <sub>S</sub> =16nH		1660		A

**Typical Performance Curves** T<sub>J</sub>=25°C unless otherwise specified



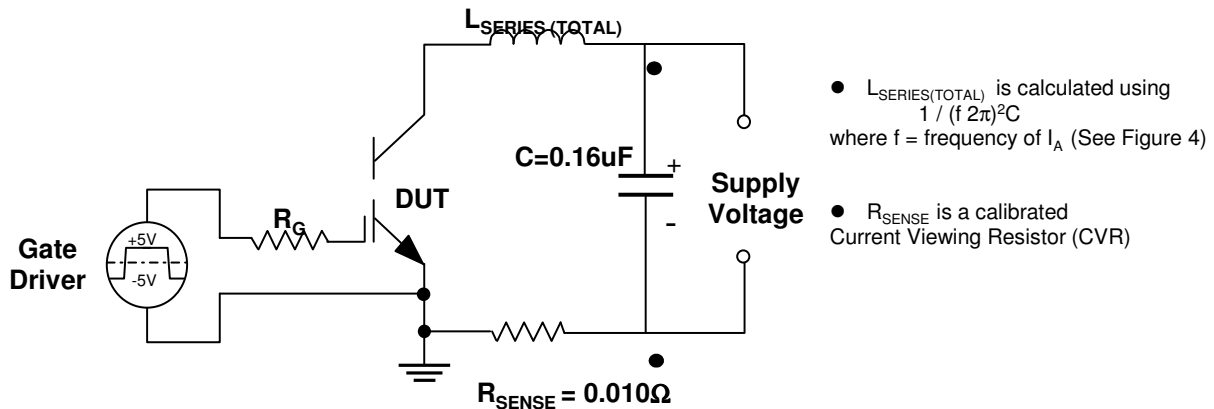
**Figure 1.** Turn-On Delay Characteristics  
 R<sub>G</sub>=3.0Ω, T<sub>J</sub>=25°C

**Typical Performance Curves (Continued)**

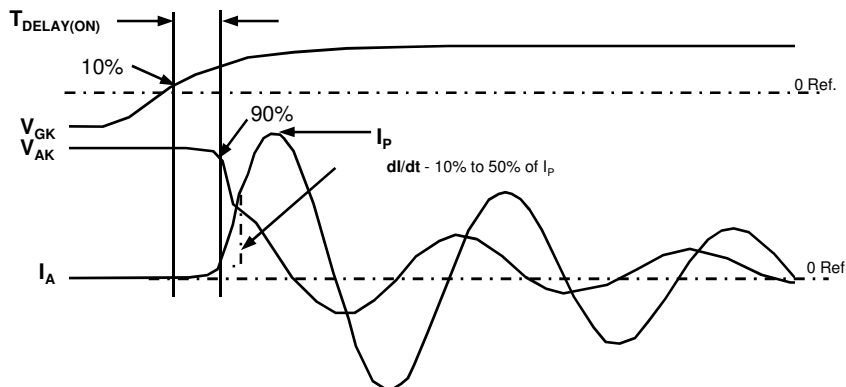


**Figure 2** On state characteristics

**Test Circuit and Waveforms**



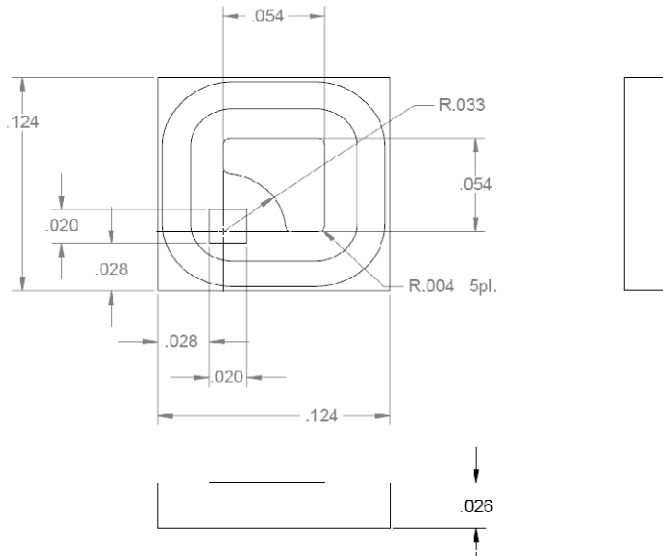
**Figure 3.** 0.16uF Pulsed Discharge Circuit Schematic



- The waveform shown is representative of one produced using a very low inductance circuit (<10nH).
- V<sub>GK</sub> is held positive until I<sub>A</sub> oscillations have ended (I<sub>A</sub>=0).

**Figure 4.** 0.16uF Pulsed Discharge Circuit Waveforms

**Package Dimensions**



All Dimensions in inch

**Figure 5.** Critical Die Dimensions

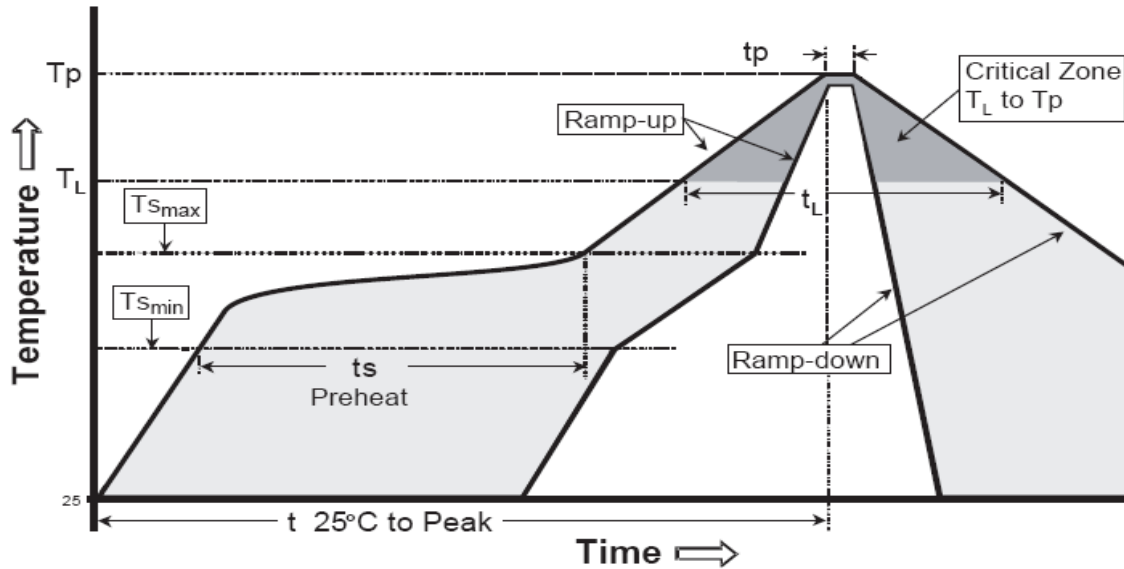
**General Handling Precautions**

1. Surface condition of the bare die prior to die attachment should be free of defects and contamination. Any contamination on the die may degrade the electrical and thermal performance of the device. Proper cleaning prior to attachment and encapsulation material is necessary to prevent arching, adhesion of the encapsulant, or solderability.
2. Proper procedures and equipment must be used when handling bare die.
3. Installation reflow temperature should not exceed 260°C or internal package degradation may result.
4. As with all MOS gated devices, proper handling procedures must be observed to prevent electrostatic discharge which may result in permanent damage to the gate of the device



'ATTENTION OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC DISCHARGE SENSITIVE DEVICES IN ALL ASSEMBLY AND TEST AREAS'

**Recommended Reflow Profile:**



IPC-020c-5-1

	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate ( $t_{smax}$ to $t_p$ )	3°C/second max.	3°C/second max.
Preheat		
Temperature Min ( $t_{smin}$ )	100°C	150°C
Temperature Max ( $t_{smax}$ )	150°C	200°C
Time ( $t_{smin}$ to $t_{smax}$ )	60-120 seconds	60-180 seconds
Time maintained above:		
Temperature ( $t_L$ )	183°C	217°C
Time ( $t_L$ )	60-150 seconds	60-150 seconds
Peak/Classification Temperature ( $t_p$ )	240 +0/-5°C	260 +0°C
Temperature ( $t_p$ )	10-30 seconds	20-40 seconds
Ramp-Down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

**Revision History**

Rev	Date	EA #	Nature of Change
0	01-08-2009	04242009-NB-0004	Initial Issue